High performance oxide thin film transistors with solution processible Cu source / drain electrode

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A high resolution (≥200 ppi) and large panel size (≥70 inch) for the next generation TFT-LCD and AMOLED display necessitates the adoption of Cu thin film as the gate and data line due to the stringent RC delay time issue. Amorphous metal oxide TFTs are able to replace the conventional amorphous Si and polycrystalline Si TFTs due to their intriguing features such as high mobility, low cost capability and good substrate scalability up to Gen. 11. Therefore, it is essential to study the oxide TFTs with a Cu electrode as source/drain (S/D). In this study, we fabricated the indium zinc oxide (IZO) TFTs with a reverse offset processed Cu S/D electrode.

A three-inch diameter InO: ZnO ceramic target (In : Zn = 6 : 4) was used as the IZO precursor. During channel deposition, the DC power to the IZO target was fixed at 100 W. The working pressure was 0.26 Pa and the relative oxygen flow rate of $[O_2]/[Ar+O_2]$ was 0.30. The Ta film was deposited on IZO channel by magnetron sputtering system. The Cu S/D electrode was patterned by reverse offset process

The control IZO TFTs exhibited the field-effect mobility (μ_{FE}) of 20.9 cm^2/Vs, subthreshold gate swing (SS) of 0.5 V/decade and threshold voltage (V_{th}) of 4.7 V. However, IZO TFTs with Ta film inserted as a diffusion barrier, exhibited the improved device performance: mobility, V_{th} and SS values were enhanced to 31.6 cm^2/Vs, 2.4 V and , 0.4 V/decade respectively. The improvement in the Ta inserted device was attributed to the suppression of Cu lateral diffusion into the IZO channel region.

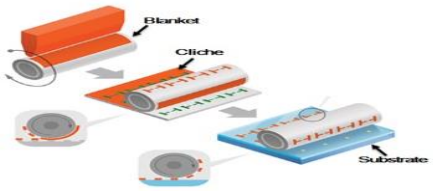

Fig. 1. Scheme of Cu reverse offset process

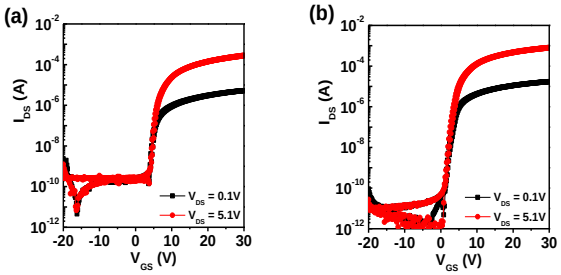

Fig. 2. Transfer characteristics of (a) without diffusion barrier and (b) with diffusion barrier

[1] Chul-Kyu Lee, Se Yeob Park, and Jae Kyeong Jeong, Phys. Status Solidi (RRL) **7**, 196 (2013).

[2] H. Ono, T. Nakano, and T. Ohta, Appl. Phys. Lett. **64,** 1511 (1994).