The Fabrication and Characterization for Top Gated Sol-Gel InZnO Transistors

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This study focuses on the fabrication and characterization for the top gated sol-gel InZnO (IZO) transistors. Oxide transistors have attracted much attention due to their superior device properties, especially low leakage current and high field effect mobility, than traditional amorphous silicon transistors in recent years. Sol-gel method for fabricating oxide semiconductor, as a low cost and large area compatible technique, has been reported many times[1-4]. However oxide Semiconductors were known as humidity and oxygen sensitive materials, an appropriate passivation layer is needed for preventing the damage from outside atmosphere. Hence in this article, several polymer materials, such as PI, PVP and PMMA were investigated to serve as the top gate insulator for sol-gel IZO transistors, in addition, providing passivation for this IZO layer. Fig. 1(a) shows the capacitance-voltage result for different polymer insulators, the cross-link PVP has the highest dielectric constant and capacitance than the others. Fig. 1(b) denotes the transfer curves for different polymer insulator IZO transistors. The PVP sample has the highest mobility ~0.108 cm^2/vs, but the largest leakage current ~2 nA. The hybrid PVP/PMMA sample has the highest on/off current ratio ~ 10^4. Although cross-link PVP is a high K polymer (ε_r ~ 6), the unreacted hydroxyl group in PVP may form the leakage paths and absorb humidity. Hence PVP/PMMA polymer was adapted and the PVP/PMMA sample achieved better properties than the others. The detail reasons would be discussed in manuscripts.

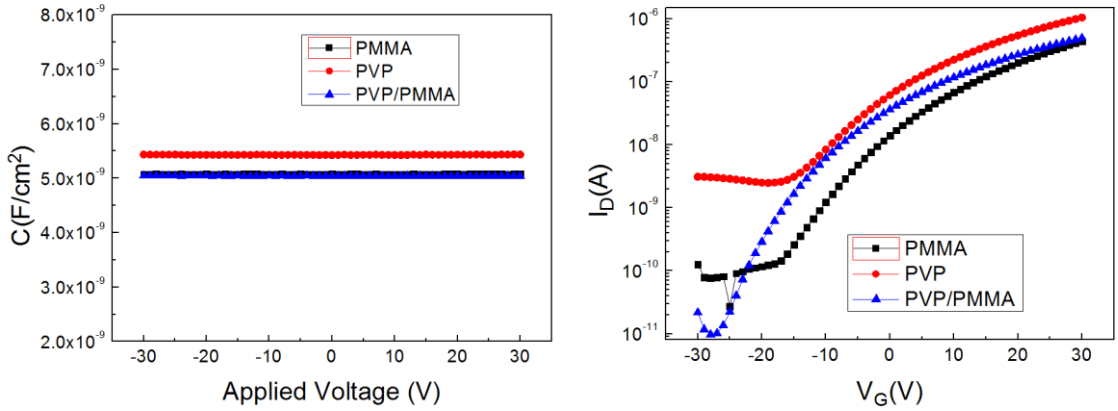

Fig. 1. (a) The Capacitance-Voltage Curves for PMMA, PVP, and PMMA/PVP insulators. And (b) Device Transfer Curves for top gated IZO transistors for PMMA, PVP and PMMA/PVP insulators.

Acknowledgment

This work was supported by the Ministry of Science and Technology, Taiwan, through Grant 103-2221-E-018-012- and Grant 103-2622-E-018-006-CC2. We acknowledge Department of Physics for providing the equipment and cooperation.

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