High Performance Sputtered High-k CLC LTPS TFTs on Glass Substrate

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Recently, low-temperature polycrystalline-silicon (LTPS) thin-film transistors (TFTs) have attracted attention in the development of small, high-resolution mobile displays. To improve the crystalline quality of thin poly-Si films, we have developed a continuous-wave laser lateral crystallization (CLC) technique using a diode-pumped solid-state (DPSS) laser [1,2]. This method enables us to achieve an n-channel mobility of 300 cm^2/Vs when silicon dioxide (SiO_2) deposited by plasma-enhanced chemical-vapour deposition (PECVD) is used as the gate stack.

The high-k gate stack may be a key technology for improving the performance of poly-Si TFTs. Further, sputtering is a standard method employed in display manufacturing. In this paper, we demonstrate the performance of CLC LTPS TFTs with a sputtered Al_2O_3 [3] and HfO_2 [4] gate dielectric. To evaluate the device performance, we measured the capacitance equivalent thickness (CET) using split capacitance-voltage (C-V) measurements with a large channel area. The physical thickness of Al_2O_3 and HfO_2 measured by transmission electron microscopy (TEM) were 20 nm and 19 nm, respectively, with a 6-nm-thick lower SiO_2 layer. For reference, CLC LTPS TFT with a 50-nm-thick SiO_2 gate stack was prepared by PECVD. The Al_2O_3 CLC LTPS TFT exhibited a field-effect mobility of 160 cm^2/Vs and an s-value of 200 mV/dec. The performances of HfO_2 CLC LTPS TFTs were almost the same as those of Al_2O_3 TFTs. The on-currents that were achieved for HfO_2 CLC LTPS TFTs were two and four times the values for Al_2O_3 and SiO_2 CLC LTPS TFTs, respectively. This was because of the high field-effect mobility, small s.s. and small CET of HfO_2 CLC LTPS TFTs. The performances of these TFTs are summarized in Table I [4]. The obtained field-effect mobility of 160 cm^2/Vs for the CLC LTPS TFT with sputtered HfO_2 is larger than those of previously reported poly-Si TFTs with high-k gate dielectrics, and this is attributed to the high-quality poly-Si film. Moreover, we realized the successful operation of a CMOS inverter with an HfO_2 gate stack at V_{dd} = 2.0 V, as shown in Fig. 1.

Table I. Performance of CLC LTPS TFTs with SiO_2, Al_2O_3 and HfO_2 gate stack

	V_{th} (V) *	S.S. (mV/dec)	CET (nm)	μ_{FE} (cm^2/Vs)	I_{on} (μA) **
SiO_2	-2.8	400	50	300	17
Al_2O_3	0.5	200	18	160	35
HfO_2	-0.9	200	11	160	65

* @10^{-9} (A) ** $V_d=V_g-V_{th}=3.0$ (V)

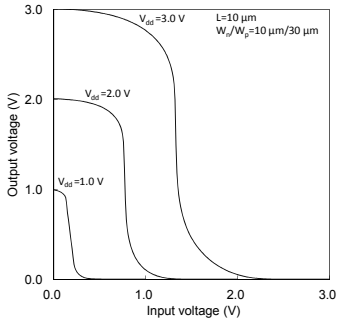

Fig. 1. CMOS inverter made up of CLC LTPS TFTs with HfO_2 gate stack.

References

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