Thermally Stable In-Ga-Zn-O Homojunction formed by Plasma Treatment with Substrate Bias for Self-Aligned Thin-Film Transistors

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An In-Ga-Zn-O (IGZO) thin-film transistor (TFT) is of increasing interest for next-generation active-matrix displays (AMDs) due to its high mobility (μ＞10cm^2/V･s), low subthreshold swing (S) values[1]. Recently, self-aligned (SA) structure is actively studied for oxide TFTs. There are several reports of IGZO homojunction with highly conductive IGZO regions, which were formed by the selective exposure of Ar, H_2, or He plasma[2]. However, it was reported that the performance of SA IGZO TFTs with source/drain (S/D) regions formed by Ar, H_2, or He plasma treatment easily degraded after thermal annealing around 200-300 °C. In this study, we present a method to enhance thermal stability of low-resistive IGZO region by applying a substrate bias during plasma treatment. The SA IGZO TFT was successfully achieved even after post-annealing at 350 °C.

Figure 1 shows the fabrication process of Hall device for resistivity (ρ) measurement. Figure 2 shows the ρ of Ar-plasma-treated IGZO films as a function of post-annealing temperature. During the Ar plasma treatment, only the substrate bias was varied from 0 to 100 W with the source plasma power of 500 W. The post-annealing was carried out in N_2 for 1 hour. For the Ar-plasma-treated IGZO film without substrate bias (P_B=0 W), ρ of as fabricated specimen (1.1×10^4 Ωcm) increased over five orders of magnitude after 350 °C annealing. On the other hand, by applying the P_B=100 W, the thermal stability of Ar-plasma-treated IGZO drastically improved, and ρ of 1.6×10^{-2} Ωcm was achieved even after the annealing at 350 °C. We found that the substrate bias during plasma treatment is an effective method to improve thermal stability of the ρ of the IGZO for S/D regions of SA TFT.

Figure 3 shows the fabrication process of bottom-gate type SA IGZO TFT. Details of fabrication process were described in our previous reports[3]. Figure 4 shows the transfer characteristics of SA-TFT after post-annealing at 350 °C. The TFT without plasma-treatment in S/D regions showed very low on-current, owing to a huge series resistance of the S/D regions. In contract, the TFT with Ar plasma treatment with P_B=100 W exhibited a drastic improvement of the drain current.

The effect of the substrate bias on thermal stability of low-resistive IGZO film will be discussed with XPS data. In addition, the result of He plasma treatment with the substrate bias will also be presented at the conference.

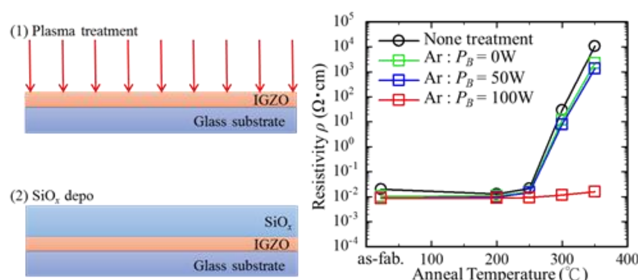

Table. 1

Resistivity (Ω・cm)	as-fab.	350℃ anneal
None treatment	2.0×10^{-2}	11×10^{4}
Ar : P_B=0W	1.0×10^{-2}	2.2×10^{3}
Ar : P_B=50W	8.8×10^{-3}	1.3×10^{3}
Ar : P_B=100W	8.7×10^{-3}	1.6×10^{-2}

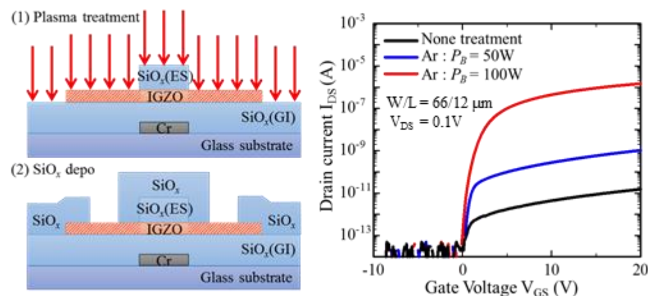

Table. 2

	Ar : P_B = 100W
Mobility μ_{lin} (cm^{2}V^{-1}s^{-1})	8.65
S (V/dec)	0.47
V_{th} (I_{DS} = 1nA)	2.07

Fig. 1 Hall device for ρ measurement.
Fig. 2 Annealing temperature dependence of ρ_{IGZO}.
Table. 1. Summary of ρ_{IGZO}.

Fig. 3. Fabrication steps of SA IGZO TFT.
Fig. 4. Transfer characteristics of SA IGZO TFTs.
Table. 2. Summary of electrical properties of SA IGZO TFTs.

References

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