Effect of interface location within solution-processed In-Ga-Zn-O thin-film transistors

Jae Won Na, Yeong-gyu Kim, and Hyun Jae Kim*
School of Electrical and Electronic Engineering, Yonsei University, 50 Yonsei-ro, Seodaemun-gu, Seoul 120-749, Republic of Korea
Tel.:82-2-2123-5865, E-mail: hjk3@yonsei.ac.kr

Amorphous oxide semiconductors (AOSs) have been attracting much attention as a next generation active layer material for thin film transistors (TFTs) in display back-plane due to their better electrical characteristics, compared with conventional amorphous Si.[1] Among many AOSs, In-Ga-Zn-O (IGZO) is emerging as a promising candidate to replace amorphous Si in TFTs. Although most IGZO TFTs are fabricated using the conventional vacuum techniques, many research groups are focusing on solution-processed IGZO TFTs due to their advantages such as low cost and simplicity in material composition. However, the solution-processed IGZO TFTs have inferior electrical characteristics, compared with the conventaional vacuum-processed IGZO TFTs. The cause for such inferiority is believed to be pin-holes and pore sites created during solvent volatilization. In order to overcome the degradation of electrical characteristics caused by pin-holes and pore sites, we previously introduced multi stacked IGZO TFT structure.[2] However, the multi stacked IGZO TFT structure inevitable creates interfaces within the active layer, and effects of the interfaces are not thoroughly studied yet. Known that molarity of IGZO precursor solution is proportional to thickness of IGZO films, we have fabricated three types of double stacked IGZO TFTs with the same thickness, using 0.05, 0.15, 0.25 M IGZO precursor solutions: top/bottom, 0.25/0.05, 0.15/0.15, 0.05/0.25 M double stacked IGZO TFTs. They have an interface at different locations within the active layer as shown in Figure 1(a)-(c). The electrical characteristics of the three types of double stacked IGZO TFTs in figure 1(d) showed an increasing tendency, as the interface moved further from the gate insulator: mobility improved from 0.35 to 1.7 cm^2/Vs, on current increased from 2.41 x 10^{-5} to 9.22 x 10^{-5} A. The 0.25/0.05 M double stacked IGZO TFT with the lowest interface location exhibited the most inferior electrical characteristics among the three types of double stacked IGZO TFTs, because the interface within the active layer acts as a electron trapping layer, hindering the transport of accumulated electrons from source to drain.

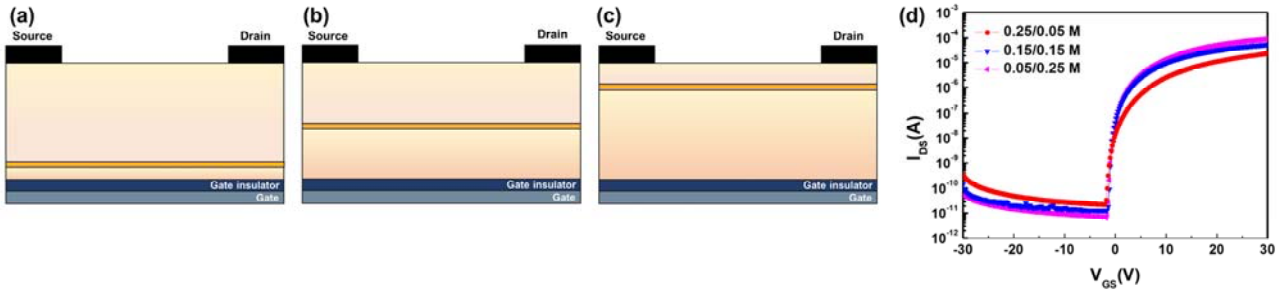

Fig. 1. Cross-sectional diagrams of (a) 0.25/0.05, (b) 0.15/0.15, (c) 0.05/0.25 M double stacked IGZO TFTs, and (d) transfer characteristics of 0.25/0.05, 0.15/0.15, 0.05/0.25 M double stacked IGZO TFTs.

Acknowledgment

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean Ministry of Education, Science and Technology (MEST) [no. 2011-0028819].

References

1. S. J. Kim, S. Yoon, H. J. Kim, *Jpn. J. Appl. Phys*., 53, 02BA02 (2014)
2. D. J. Kim, D. L. Kim, Y. S. Rim, C. H. Kim, W. H. Jeong, H. S. Lim, H. J. Kim, *ACS Appl. Mater. Interfaces*, 4, 4001-4005 (2012).