Novel approach self-positioning of organic semiconductor with large grain size on a bottom contact structure TFT during solution jetting process

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We investigate the self-positioning ink-jet technique of soluble organic semiconductor with P-29-DPPDTSE by using double layered drying (DLD) method. The DLD process with heterogeneity solvent system for a soluble processible organic semiconductor (s-OSC) on organic gate insulator (GI) is developed.

In this study, s-OSC self-positioning technique is examined for obtaining accurate position and well-ordered grain growth during the DLD method ; we used the P-29-DPPDTSE as an OSC and octadecyl trichlorosilane (OTS) as a selective area self assembled monolayer (SAMs) method on GI with DLD. We obtained acurate position and large-sized grain of P-29-DPPDTSE when the OSC solution was jetted on the gate insulator (GI) covered with fluoro-anti-solvent, which separate the OSC ink from gate insulator surface.

OTFTs with bottom gate and bottom contact (BG-BC) structure are used to confirm the effect of DLD method. OTFTs' structure was bottom contact configuration with organosiloxane-based hybrimer (named as EK8). The gold S-D electrodes and SAMs treatment were patterned with conventional photolithography method; width (W) were 500μm and length (L) of OTFTs were 300 and 400μm. P-29-DPPDTSE was jetted micro pipet. Device exhibited improving characteristics in terms of a threshold voltage of -3.0V (below), a sub-threshold slope of 0.7 V/dec and a field-effect mobility of 3.0 cm^2/Vs.

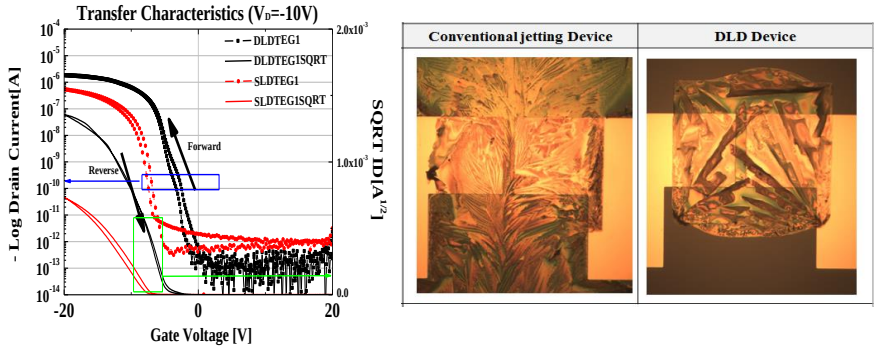

Fig. 1. Example of transfer characteristic (a) and optical image of OFETs(b)

	V_{TH}	Subthreshold slope	Mobility μ
Conventional Device	-7.4 V	0.264V/dec	0.034cm^2/V.s
DLD Device	-4.54V	0.395V/dec	0.64cm^2/V.s

Table I. Typical parameters of present TFTs.

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References

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