Organic thin-film transistors employing hybrid bilayer gate dielectric for AMOLED displays

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There have been reports to explore to high-performance organic thin-film transistors (OTFTs) for the display backplanes. One promising approach is based on careful choice for a gate dielectric which determines the interfacial characteristics in OTFTs [1]. Suitable combination of high-k and low-k dielectrics into devices can be a challenge towards further practical advances of AMOLED displays [2].
Hysteresis caused by charge trapping/de-trapping at the semiconductor/dielectric interface or in a dielectric along with the sweep of applied gate voltage in OTFTs, leads to failure in operation of high quality AMOLED displays [3]. Commonly, a large hysteresis window has been reported in OTFTs due to the hydroxyl and water molecules as trapping/de-trapping centers [4]. Since high-k dielectrics increase the density of trap states as well as induce strong polarization in OTFTs, comprehensive investigation on mechanism of hysteresis characteristics can be the key to better understanding of charge transport and device perforamance.
In this presentation, we demonstrate solution-processed hybrid bilayer gate dielectrics on device performance and electrical instability in OTFTs. Optimized OTFT devices exhibit improvement in all device key metrics such as field-effect mobility, on-off current ratio, threshold voltage and sub-threshold swing. We also discuss enhanced stability against electrical bias-stress and hysteresis-free characteristics in both dark and illuminated measuring conditions in OTFTs.

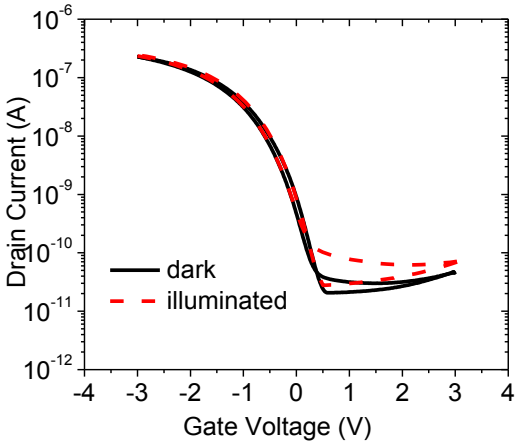

Fig. 1. Hysteresis in OTFT employing hybrid gate dielectrics in both dark and illuminated measuring conditions.

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