Volume Transport in Dual-Gate Thin-Film Transistors Using Ultra-Thin Amorphous Oxide and Polymer Semiconductors

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The display industry is fast evolving for the ceaseless demand for large area, flexible, low power consumption, high resolution, and low cost applications, which has stimulated the introduction of new switching devices to replace the present silicon-based technologies. Metal oxide and organic thin-film transistors (TFTs) are believed to be promising in this respect. These new devices, however, may still suffer from low performance and poor stability as well as large parameter variations particularly for those manufactured by solution-based processing. In this work, we present that dual-gate (DG) TFTs can offer a great opportunity to overcome such issues and thus enable their practical use in future displays.

Fig. 1 shows the simulation results of two DG IGZO TFTs having different semiconductor thicknesses. One can readily recognize the difference: electron accumulation is only at the two surfaces for 100 nm-thick IGZO yet as the thickness is reduced to 10 nm the charge transport extends into the entire film thickness due to electrical field coupling of the two gates inducing volume charge transport in semiconductor bulk. Compared to surface counterpart, volume transport is less susceptible to the detrimental influences arising from the contacting gate dielectrics and their interfaces, i.e., being more intrinsic with superior carrier mobility, stability, and uniformity. Meanwhile, full depletion can lead to very low off current that is instrumental to reducing power consumption and improvement of dynamic spanning. By incorporation of ultra-thin films of amorphous oxide and polymer semiconductors, we show that efficient volume transport can be achieved in dual-gate TFTs and the underlying mechanisms are also revealed.

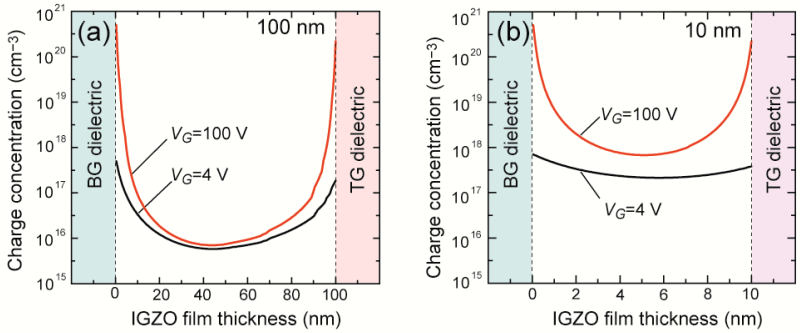

Fig. 1. Simulated charge distribution profile in two dual-gate transistors with IGZO film thickness of 100 nm (a) and 10 nm (b), where BG and TG dielectrics represent the bottom-gate dielectric (300 nm SiO_2) and the top-gate dielectric (500 nm PMMA), respectively.

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