Positive Bias Stress Stability in Solution Processed Top-gate and Top-contact a-IGZO Thin Film Transistors

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The oxide thin-film-transistors (TFTs) have been a very attractive research area for the flat panel displays such as active matrix liquid crystal displays and organic light emitting diode displays [1]. However, solution-processed oxide TFTs exhibit poor stability under positive bias stress (PBS). Solution-processed oxide TFTs have two typical defects, which are intrinsic oxygen vacancy and organic chemical induced defects [2-4]. In this study, the top-gate and top-contact IGZO TFTs were fabricated on glass substrates with spin-coated IGZO film. The Al source/drain electrodes were deposited by thermal evaporation. On top of the source/drain, PMMA (poly(methyl methacrylate)) was spin-coated to a thickness of 180 nm. The PMMA layer has a dual role. It works as a gate insulator, and also acts as a channel passivation layer. The channel passivation layer suppresses the electric-field-induced threshold voltage instability which is caused by the adsorption of oxygen and water molecules from the atmosphere. The gate electrode, a 100 nm thick Al layer, was deposited through the shadow mask by thermal evaporation.

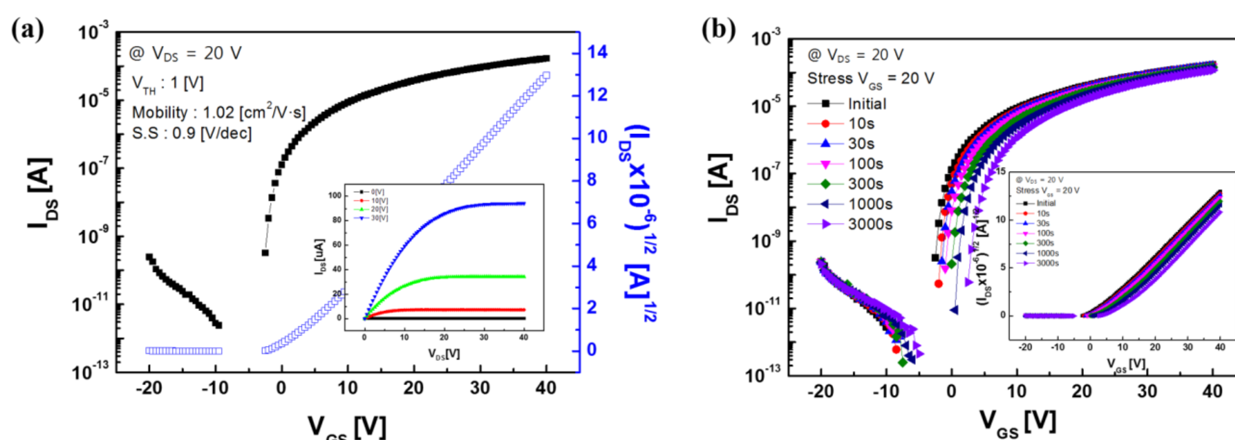

Fig. 1. Transfer characteristics of IGZO TFTs (a) Initial performance (Inset: output characteristics) (b) various bias stress time (Inset: $(I_{DS})^{1/2}$ versus V_{GS})

Fig. 1(a) shows the transfer characteristics of IGZO TFTs where the V_{GS} was swept from -20 to 40 V with the sweep step of 0.5 V at the V_{DS} of 20 V. From the experimental data, a field-effect mobility (μ_{FET}) of 1.02 $cm^2/V \cdot s$, a V_{TH} of 1 V, on/off current ratio of > 10^7 and sub-threshold slope of 0.9 V/dec can be estimated for the IGZO TFTs. The inset shows the output characteristics of IGZO TFTs. Fig. 1(b) shows the transfer characteristics of IGZO TFTs at the initial and after positive bias stress for various times. Before the bias stress, device had a threshold voltage of 1 V and after bias stress time of 10, 30, 100, 300, 1000 and 3000 sec an increased V_{TH} of 2, 3, 4, 5, 6.5, 8.5 V, respectively was obtained. The transfer curves shifted towards the positive direction. The phenomenon of the ΔV_{TH} shift can be explained using an electron charge trapping mechanism. The ΔV_{TH} is caused by the trapping of charges in traps, located at the interface and dielectric layers.

References

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