

## A Low-Jitter and High-Speed LVDS Receiver Using Data-Dependent Jitter Compensation

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Recently, as the size of video becomes larger and the resolution of display increases, a required bandwidth of display interface becomes wider. To achieve a wide bandwidth with low power consumption, a multichannel LVDS (low voltage differential signaling) has been widely used for a display interface. However, it requires several redundant blocks such as skew compensation circuits, and moreover occupies a large chip area to sense and recover the data and clock synchronization. A transceiver which can transfer the data over 2 Gbps per channel was reported in [1], but consumes a large power. To solve the above problems, we propose a new scheme of receiver circuit for the LVDS display interface.

Fig. 1 shows the schematic diagram of the proposed LVDS receiver with the differential-to-single-ended (D2S) conversion stage including MPF1 and MPF2. In the conventional receiver without MPF1 and MPF2, it typically takes several data unit intervals (UIs) to reach the maximum voltage ( $V_{DD}-V_{TH}$ ) at the drain voltage of MP8 ( $V_3$ ), since the pull-up current of MP8 decreases as the voltage of  $V_3$  increases, as shown in Fig. 2(a). Since the voltage of  $V_3$  is determined by the input data pattern until  $V_{P2}$  becomes high, the voltage difference of  $V_3$  at the end of T1 and T2 causes the data-dependent jitter of  $V_{OUT}$ . To reduce the data-dependent jitter, MPF1 and MPF2 are used in the proposed LVDS receiver. When  $V_{P2}$  is low, MPF1 is turned on and the voltage of  $V_3$  pulls up to  $V_{DD}$  within one UI as illustrated in Fig. 2(b), and thereby the voltage of  $V_3$  becomes independent of the input data pattern, which results in the data independent jitter of  $V_{OUT}$ . MPF2 is added to balance the load of the input stage and enhance the pull-up strength of the D2S stage.

To verify the performance of the proposed receiver, the HSPICE simulation is performed using 0.18- $\mu\text{m}$  CMOS process with 1.8 V supply voltage. In the simulation results, the proposed receiver shows the peak-to-peak jitter of 7.0 psec and the power consumption of 0.8 mW at the input data rate of 1.6 Gbps. Compared with [2], the proposed receiver has a half of the jitter and about one third of the power consumption. Also, at the input data rate of 700 Mbps, the conventional receiver [3] shows the peak-to-peak jitter of 8.13 psec at the rising edge of  $V_{OUT}$ , whereas the proposed receiver has the peak-to-peak jitter of only 1.12 psec, which is reduced by 86.23% compared with [3].

In this paper, we propose the LVDS receiver to reduce the data-dependent jitter by increasing the pull-up current of the D2S stage. The proposed LVDS receiver can be applied to a low-jitter and high-speed display interface so that the data rate of display interface can be increased while lowering power consumption.

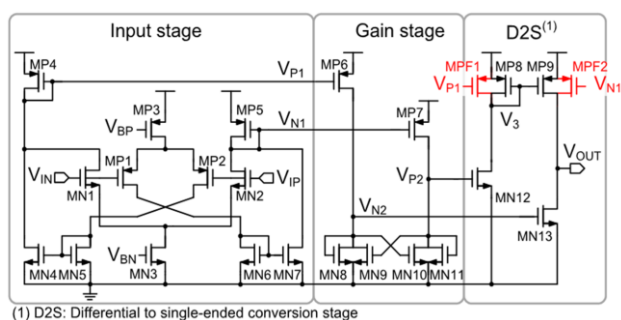


Fig. 1. Schematic diagram of the proposed receiver

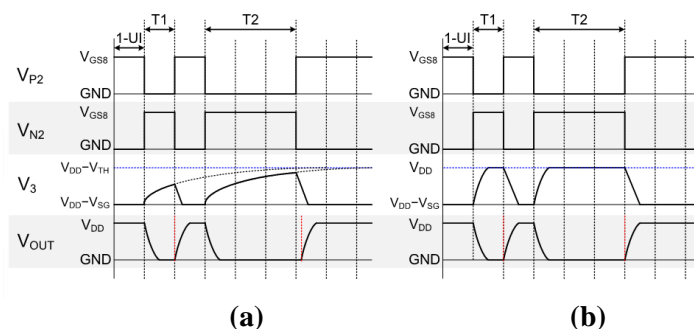


Fig. 2. Waveforms of D2S stages of (a) the conventional receiver [2] and (b) the proposed receiver.

### References

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