A 10-bit Two-Stage DAC with an Area-Efficient Decoder for Flat Panel Display Source Driver ICs

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Recently, several small-area digital-to-analog converts (DACs) with high-resolution have been researched to achieve high color depth active matrix flat panel displays (AMFPDs). Among the DACs, a two-stage DAC has been commonly adopted to reduce the area of source driver IC, but still needs a large number of transistors in the first-stage DAC to transfer two adjacent voltages to the second-stage DAC [1-2]. To solve the above problem, we propose a new DAC structure which requires less number of transistors than the conventional DACs.

Figure 1 (a) shows the simplified schematic of the proposed DAC with 3-bit resolution. The proposed first-stage DAC structure is divided into three parts: a tree-type decoder, a proposed area-efficient decoder, and a selector for high level output voltage (V_H) and low level output voltage (V_L). Firstly, the tree-type decoder with 2-bit resolution selects one of the odd-numbered reference voltages (V_1, V_3, V_5, and V_7) for the first output voltage (V_{OUT1}) using 2-bit digital signals (b_1 and b_2). Secondly, the proposed decoder selects one of the even-numbered reference voltages (V_0, V_2, V_4, V_6, and V_8) for the second output voltage (V_{OUT2}) using c_0 - c_2 and b_2, where c_0 - c_2 are three additional control signals generated by b_0 and b_1 as shown in Figure 1 (a). As a result, the proposed DAC uses less number of transistors than conventional DACs. Finally, the selector transfers the outputs of the first-stage DAC (V_{OUT1} and V_{OUT2}) to inputs of the second stage DAC, and determines V_H and V_L according to the least significant bit (LSB), b_0.

Figure 1 (b) shows the chip microphotograph of 20 channel source driver IC which is fabricated using a 0.18-μm CMOS process with 1.8 V and 18 V CMOS devices. The proposed 10-bit two-stage DAC occupies 713 × 33 μm^2 and its measured integral nonlinearity (INL) and differential nonlinearity (DNL) are 0.487 LSB and 0.089 LSB, respectively.

In this paper, we propose a 10-bit two-stage DAC for high color depth AMFPDs. The proposed DAC achieves a small area and high resolution by adopting an area efficient decoder which simplifies the selection procedure of the reference voltage.

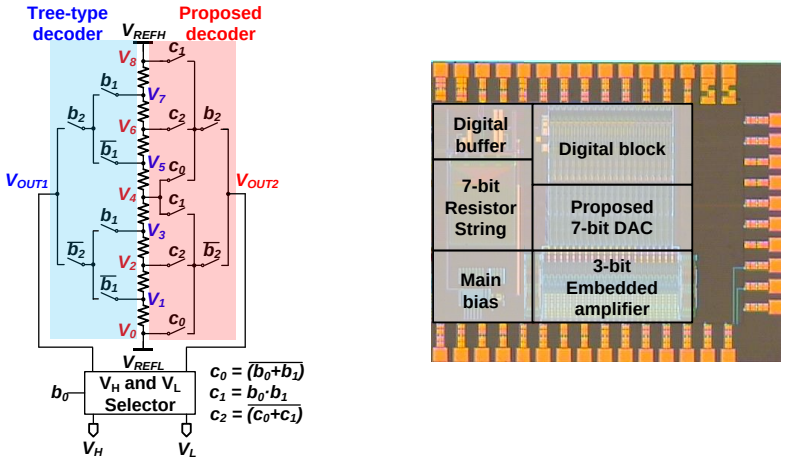

Fig. 1 (a) Simplified schematic of the proposed first-stage 3-bit DAC and (b) chip microphotograph of 20 channel source driver IC

References

1. S. Lan and T. Teraishi, U.S. Patent 7 006 027 (2006)
2. C.-W. Lu, C.-M. Hsiao and P.-Y. Yin, IEEE J. Solid-State Circuits, Vol. 48, pp. 1475-1486 (2013)