DC-type output driving scheme for low power LTPS TFT gate driver circuit

Seok-Jeong Song, Byung Hoon Kim, and Hyoungsik Nam
Dept. of Inform. Display, Kyung Hee University, Seoul 130-701, Korea
Tel.:82-2-961-0925, E-mail: hyoungsiknam@khu.ac.kr

This paper demonstrates a low power DC-type low temperature poly-Si (LTPS) thin-film transistor (TFT) shift register that consists of nine TFTs and one bootstrapping capacitor. The proposed circuit connects large size pull-up TFTs of output drivers to positive supply instead of alternating clock signals in order to reduce substantially the power consumption of clock drivers [1-2]. The SPICE simulation ensures that the variable overlap intervals can be programmed by the delay between clock signals and the overall power consumption of a DC-type circuit can be reduced to 45 % of an AC-type one for a full-HD display. The operation of a proposed structure is also verified with a fabricated 16-stage gate driver.

Fig. 1(a) shows the schematic of a proposed DC-type shift register which is made up of nine n-channel LTPS TFTs (T1-T9) and one bootstrapping capacitor (C1). The pull-up TFT of an output driver (T8) is not connected to any alternating clock signals, but to the positive supply voltage (VGH). The operation of the circuit is controlled by four clock signals (CLK1, CLK1b, CLK2, CLK2b). As depicted in the timing diagram of Fig. 1(b), CLK1b and CLK2b are the out-of-phase clocks of CLK1 and CLK2, respectively, where CLK2 is a delayed one of CLK1 by Td. The pulse width of clock signals is set to one line time.
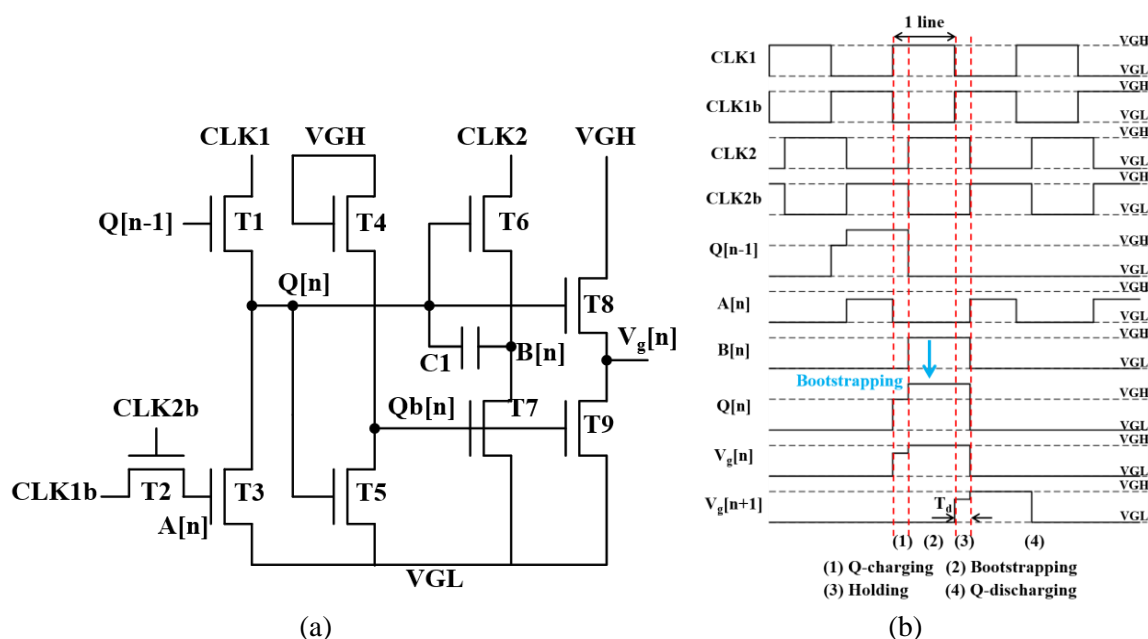

Fig. 1. Proposed DC-type LTPS TFT shift register (a) schematic (b) timing diagram

Acknowledgment

References

1. M. Nakamizo, M. Yonemaru, Y. Iwase, and T. Fukaya, *SID'10 Technical Digest*, Vol. 1, p. 28 (2010).
2. S.-J. Yoo, S.-J. Hong, J.-S. Kang, H.-J. In, and O.-K. Kwon, *IEEE Electron Device Lett.*, 33(3), 402 (2012).
3. E. Song and H. Nam, *J. Soc. Info. Display*, 22(1), 18 (2014).
4. E. Song and H. Nam, *J. Display Technol.*, 10(10), 834 (2014).