Flicker Analysis with RC Delay by using Behavioral Circuit Model

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For much higher and advanced performance of active matrix liquid crystal displys(AMLCDs) such as flicker, uniformity, and so on, electrical and optical characteristics of liquid crystal (LC) should be accurately predicted [1]. In order to acheve it, we sucessfully developed a behavioral circuit model of AMLCDs by applying a first-order circuit system [2]. We presented accurate optical responses of AMLCDs of twisted-nematic (TN), in-plane switching (IPS), and patterned vertical alignment (PVA) modes [2]. In this work, we analysis the flicker depending on the V_{com} level and RC delay of signal lines by using the behavioral circuit model.

A 40 inch, FHD (1920 × 1080), 120Hz LCD panel was used for our simulation. The pixel charging time of the panel was about 7.7 μs. In order to investigate the flicker level depending on V_{com} levels and RC conditions, we selected five positions on the LCD panel as shown in Fig. 1(a). As shown in Fig. 1(a), the position *"A"* is less affected by RC delay because it is located in the proximity of gate and data driver ICs. The farther position from the gate or data driver ICs such as positions *"B"* or *"D"*, however, the worse gate or data signal distortion occurs, respectively. In Fig. 1(a), the total RC delay times for the gate and data line were about 2 μs and 1 μs, respectively. Fig. 1(b) shows the simulation results of the flicker at position *"A"* when V_{com} is 4.7V. We calculated the flicker level as $\text{Flicker} = (T_{\max} - T_{\min}) / T_{aver}$. Here, T_{max}, T_{min}, and T_{aver} represent maximum, minimum, and average transmittance, respectively. T_{max}, T_{min}, and T_{aver} were about 0.41, 0.25, and 0.3, respectively as shown in Fig. 1(b). Thus, flicker level was about 53%. In this way, we compared flicker levels depending on V_{com} and RC delay levels. As shown in Fig. 1(c), V_{com} varied from 4.7V to 5.3V. In Fig. 1(c), five curves represent positions *A*, *B*, *C*, *D*, and *E*. As shown in Fig. 1(c), we can find that the optimized V_{com} is about 5V. In addition, we can find that the flicker levels are significantly affected by RC delay levels. We believe that we can apply our behavioral model to ultra-large LCD panels to predict electrical and optical performance of them. We also believe the model can evaluate driving technologies to improve optical characteristics of LCD panels.

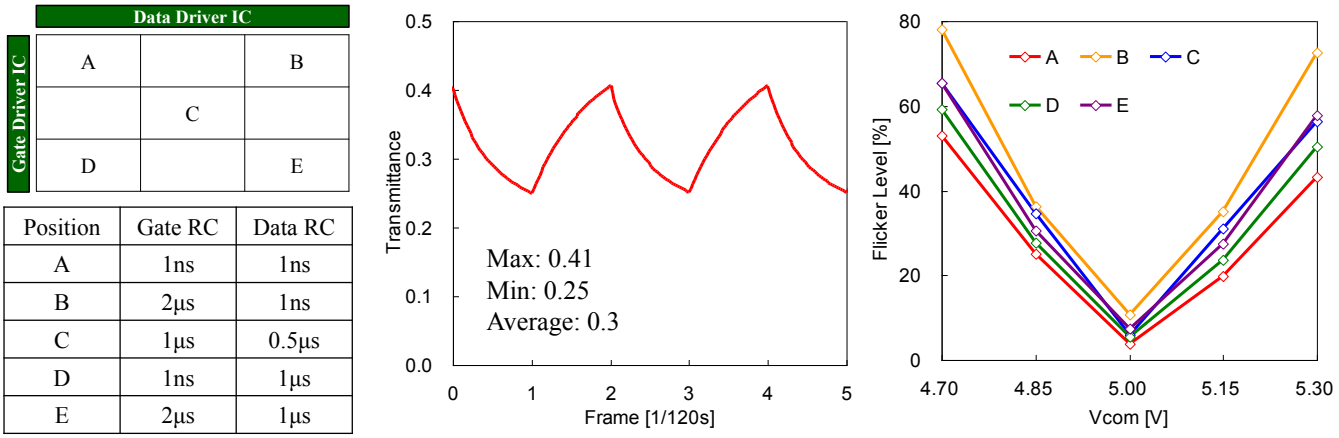

Fig. 1. (a) Selected five positions and RC delays for simulation, (b) simulation results of flicker level at position A with V_{com} = 4.7V, and (c) flicker levels depending on V_{com} and location on the screen.

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References

1. S. W. Lee, "Common voltage control technology for highly reliable active matrix liquid crystal displays," *Optical Engineering*, vol. 47, no. 2, p. 024001 (2008).
2. J. M. Kim et. Al., "Precise prediction of optical responses of all types of liquid crystal displays by behavioral models," *Journal of Society for Information Display*, vol. 21, no. 1, pp. 2-8 (2013).