An Optimal ASG Driver Circuit with New Multi-Level Clock Driving Technique

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For the display panel, the correct pixel data voltage is the most important factor of amorphous silicon gate (ASG) driver circuit [1-3] which depends on short falling time and minimal ripple to reduce the misoperation of pixel data voltage. In this work, a new ASG driver circuit's dynamic characteristic is optimized, where the explored circuit is consisting of 14 hydrogenated amorphous silicon TFTs, as shown in Fig. 1. For large panel application, the dynamical properties of the circuit is optimized for the given specifications of the fall time < 3 s and the ripple voltage < -9 V with minimizing the total layout area. Figure 2 shows the timimig flow chart, and using the new 3-level clock let the power consumption reduced in pre-charging state. Figure 3 shows a Sample and a SEM plot of the fabricated a-Si:H TFT. Figure 4 indicates the output waves between the original design and optimized result, and the falling time can have 50% reduction. And then, we compare the simulation results of the layout of the gate driver circuit with the pre-sim result. Table I shows the achieved data of the simulation and measurement, where the optimization result is better than the original design, and the measurement result is similar to the simulation result. In addition, the total width of layout also reduced after the optimizztion. Figure 5 shows the fourth stage output wave of the measurement. The ripple peak voltage of the measurement is smaller than that of the pre-simulation, because of the parasitic resistances and capacitances of the layout, but it does not have great impact of the gate driver circuit. In summary, we can confirm that the proposed gate driver circuit with the new 3-level clock driving methodology can minimize the misoperation of the correct pixel data voltage for the panel contrast.

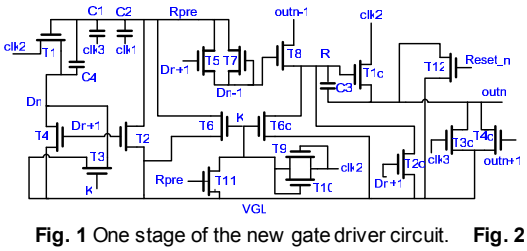

Fig. 1 One stage of the new gate driver circuit.

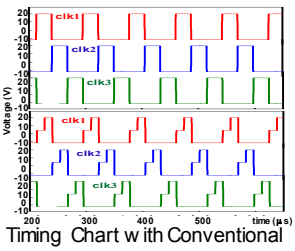

Fig. 2 Timing Chart with Conventional clock and 3 Level clock.

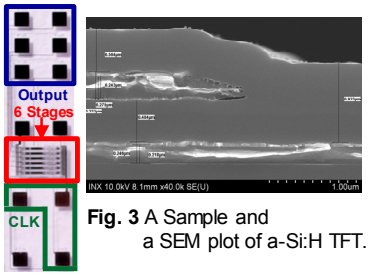

Fig. 3 A Sample and a SEM plot of a-Si:H TFT.

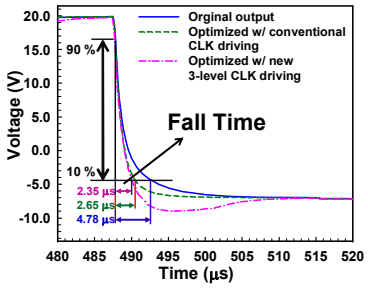

Fig. 4 The output wave of simulation.

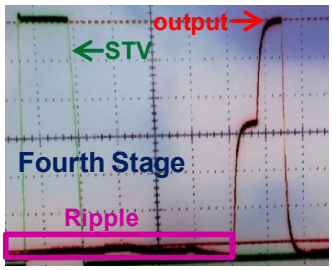

Fig. 5 The output wave of measurement.

Table I Results of simulation and measurement.

	Target Spec.	Original Design	Optimization w/ New 3-Level CLK. Driving
Simulation			
Ripple Peak (V)	<-9	-8.81	-9.96
Falling Time (μs)	< 3	4.78	2.35
Measurement			
Ripple Peak (V)	<-9	-	-11.3
Falling Time (μs)	< 3	-	2.48
Total Width (μm)	-	2846	2641

Acknowledgment

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