Top gate structured inverters with solution processed IGZO and PMMA

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Inverter with bottom gate and solution processed IGZO thin film transistors (TFTs) have proven to be reliable by many research groups [1]. In general, an inorganic passivation layer such as SiO_2 and SiN_x is used to prevent the defect of oxide TFTs in open environment, which increases the cost and time.

In this study, we designed inverter with top gate structured thin film transistors. The TFTs were fabricated by spin coating a-IGZO and PMMA on SiO_2, which reduces the process steps and fabrication cost [2]. The PMMA layer has a dual role in top gate structure. It works as a gate insulator and also as a channel passivation layer. The channel passivation layer suppresses the electric-field-induced threshold voltage instability, which is caused by the adsorption of oxygen and moisture molecules from the atmosphere. Also, the top gate structure protects the PMMA film from 2-methoxyethanol present in the IGZO solution. Figure 1(a) shows the schematic of TGBC type TFT used in the inverter and Fig. 1(b) represents the circuit diagram of enhancement mode inverter. The channel width/length ratios (W/L) of load and drive TFTs were 600/100 μm and 6000/100 μm, respectively. The enhancement mode inverter showed a gain of 2.08, output high voltage (V_{OH})= 25 V, output low voltage (V_{OL})= 4.2V, input high voltage (V_{IH})= 0V, input low voltage (V_{IL})= 10 V, and V_{th}= 5V at V_{DD}= 30 V and sweep V_{In}= -30 to 30 V. The V_{OH} of inverter is low because of the voltage drop by load TFT's threshold voltage and trapping of electron between the PMMA and the IGZO. The voltage drop in the on-state of drive TFT can be analyzed from the ratio of the resistance of load TFT and drive TFT.

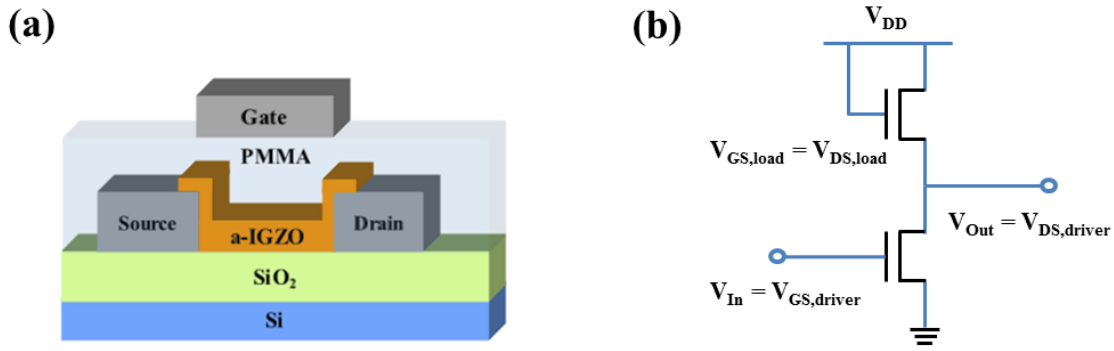

Fig. 1. (a)Top gate Bottom contact TFT structure in inverter
(b) Enhancement mode inverter circuit

References

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