TFT-Circuit-Simulation-Based Multi-objective Evolutionary Algorithm for Dynamic Specification Design Optimization of ASG Driver Circuits

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In recent years, the gate driver circuit with amorphous silicon TFT is one of the key issues of TFT-LCD panel manufacturing. To get the correct pixel data voltage and reduce the power consumption and areas, we optimize the ASG driver circuit's dynamic characteristic by using TFT circuit-simulation-based multi-objective evolutionary algorithm (MOEA) [1] on the unified optimization framework (UOF) [2], in this work. The UOF is a flexible interface to implement the MOEA optimization method to design the ASG driver circuit (Fig. 1) with the most suitable parameters [3-4]. Fig. 2 shows the block diagram of the proposed TFT circuit-simulation-based MOEA optimization method running on the UOF. The main program of UOF manages the data flow among the problem, simulator, MOEA, and optimization programs. First, according to the parameter range, the populations are randomly generated. Then, we input the data to the TFT circuit simulator and calculate the performance of designs. The optimization algorithm determines and selects superior solutions. Iteration is complete when all populations are all calculated and the fitness is assigned by MOEA. At the beginning of next iteration, we select half of the populations as parents by competition. As shown in Fig. 1, the circuit used in a large panel is optimized for the rise time, fall time, ripple waveform, total TFT widths and clock Ctotal. Table 1 lists achieved specifications and reductions. Notably, the minimum VGH which relates to the stability of circuit can be maintained for production. Fig. 3 is the waveform between the original and optimized results. The decision space generated by MOEA selection, shown in Fig. 4, projects general trend of the optimal solutions. Layout among optimize results is drawn in Fig. 5.

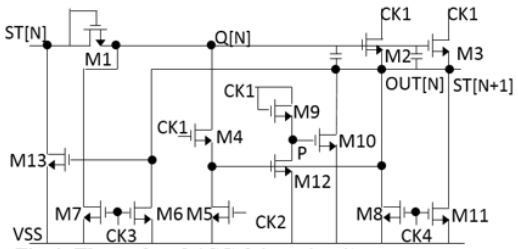

Fig. 1. The explored ASG driver circuit.

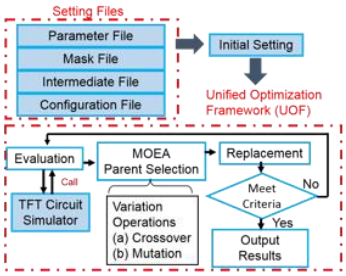

Fig. 2. A Flowchart of the proposed optimization methodology.

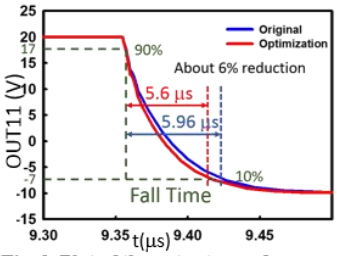

Fig. 3. Plot of the output waveforms between original and optimized results.

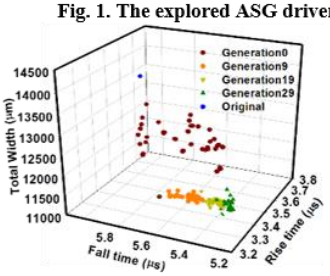

Fig. 4. Decision space among the fall time, the rise time, and the total width.

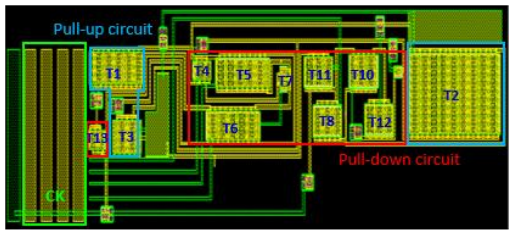

Fig. 5. Plot of the layout for the optimized ASG driver circuit.

Table 1. Comparison between the original and optimized results.

	Spec	Original Stage 11	Optimization Stage 11	Reduction	Post-Simulation
Rise time (µs)	< 4	3.63	3.57	2%	3.69
Fall time (µs)	< 5.5	5.96	5.6	6%	5.85
Ripple (V)	< 1.2	1.23	1.12	10%	0.99
Total Width (µm)	< 12000	13550	11870	12.4%	11870
CLK Ctotal (pf)	< 25	25.8	22.86	11.4%	20.9
Min VGH (V)	< 2	Vgl = -10 Vgh = 0	Vgl = -10 Vgh = 0	maintain	Vgl = -10 Vgh = 0

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References

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