A Novel Pull-Down Structure for High-Performance ASG Driver Circuits

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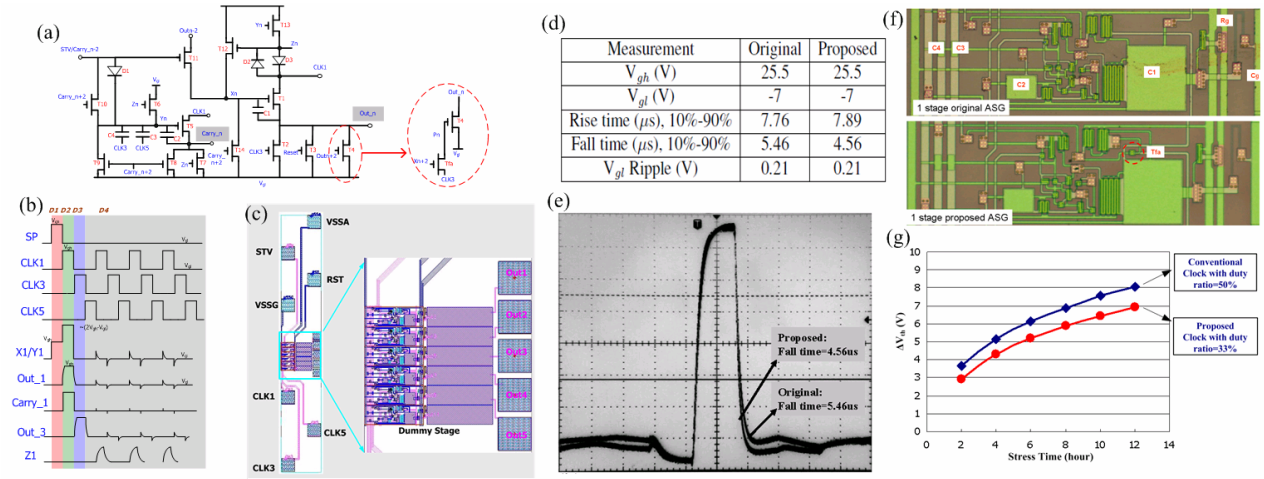
For nowadays advanced liquid crystal display (LCD) applications, the amorphous silicon gate driver (ASG) circuits embedded in a display panel become main stream [1-4]. Proper fall time of the gate output makes the pixel TFTs to be charged with correct data voltage in time. However, a long fall time may cause incorrect data voltage to the pixel TFT. In this work, we report a novel ASG circuit. In this structure, the measured fall time of the designed and implemented circuit is 17% shorter than that of the original one. Notably, the total layout area of the explored ASG driver circuit is almost invariable relatively.

As shown in Fig. 1(a), as a symbolic representation, the single stage ASG circuit is composed of seventeen TFTs and four capacitances with three external clock signals. By importing the internal signals to enhance the discharging capability of the pull-down TFT, the fall time could be reduced effectively. The relative timing chart is shown in Fig. 1(b). In order to retard the V_{th} shift effect, the 3-phases clocks were applied in the circuit. The 6-stages circuit whose layout is shown in Fig. 1(c) was fabricated using a 5-mask process. Each output was connected to a resistance (1.35 KΩ) and a capacitance (75.5 pF) as loading. The measurement data of the circuits are listed in Fig. 1(d). As we can see that their performances are almost identical except the important characteristic, the fall time, is 17% shorter than that of the original one. The realistic output waveforms between the original and proposed circuits are observed from Fig. 1(e). Besides, the layout areas are identical in both circuits as shown in Fig. 1(f). In order to verify the 3-phases clock that can alleviate the V_{th} shift, measuring the V_{th} shift values every two hours for the clocks with different duty ratios as shown in Fig 1(g). After 12-hours high-temperature (60°C) stressing, the magnitude of V_{th} shift under the clock with 33% duty ratio was about 6.9 V that was smaller about 15% than that (8.1V) of the clock with 50% duty ratio.



Measurement	Original	Proposed
V_{gh} (V)	25.5	25.5
V_{gl} (V)	-7	-7
Rise time (μs), 10%-90%	7.76	7.89
Fall time (μs), 10%-90%	5.46	4.56
V_{gl} Ripple (V)	0.21	0.21

Fig. 1. (a) The applied ASG circuit. (b) The timing chart of the proposed 3-phase clocks (c) The layout of the 6-stages ASG circuit with integrated RC loading. (d) The measurement data of the implemented samples. (e) The fall time of the original circuit was 5.46 μs and the proposed one was 4.56 μs in the measured waveforms. (f) The optical photo of the original and proposed ASG circuits. (g) The V_{th} shift measurement of two clocks biasing with different duty ratio for an a-Si:H TFT under the temperature (60°C) in 12 hours.

References

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