

Research on Line Image Sticking for Large Size High Resolution TFT-LCD Panel

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Abstract

Large size, high resolution TFT-LCD panel get a series of problems. One of the most serious problems is line image sticking. This article analyses the causes, proposes improvement for line image sticking; and conducts tests including timing adjustment, driving voltage debugging to verify the feasibility.

Author Keywords

Line Image Sticking; TFT-LCD; Large Size; High Resolution;

1. Introduction

Large size, high resolution TFT-LCD panel is worldwide welcome for their getting good pictures. However, as the size and resolution increases gradually, the single pixel charging time is becoming shorter, and therefore causes a series of problems. One of the most serious problems is line image sticking.

"Image Sticking" is image residual, usually can be shown as "Area Image Sticking" and "Line Image Sticking". Cause the essence of the two is consistent, that is, when the TFT-LCD screen for a long time to keep a static picture, the liquid crystal molecules, due to the long time drive by polarization, resulting in the liquid crystal molecules can't normal deflection under the voltage control signal. That is to say, even change the content of the display screen, the screen can still see the trace of still images^[1,2].

Image sticking is a big problem in the process of liquid crystal display manufacturing. Generally, people would like to discuss it in ion model way. When the liquid crystal cell contains impurities ion, after a long period of time fixed display the same picture, ion in the liquid crystal cell move along the electrode direction, when the ions gathered enough to affect the driving LCD voltage, will make transmittance of the liquid crystal cell changed; If switch display picture at this time, the ion has gathered cannot leave immediately from the PI surface, we will continue to see the different transmittance in the different area, resulting in image sticking^[3].

The root causes of image sticking is ions in LCD panel, at the same time, driving signal waveform distortion or contain certain DC component. Improve image sticking can start from the impurity ions, can also, from the perspective of the drive circuit^[4,5]. This article will select 65 inch UHD panels, driven structure by 2G2D, from the principle analysis, test validation, timing adjustment, driving voltage, etc, puts forward the effective improvement method, and the analysis conclusion is verified by the actual result, provides a feasible improvement measures for the large size, high resolution product line image sticking problems.

2. Driving Principle Analysis

Based on the above systems, this article mainly discussed from the following several aspects:

2.1. The Influence of The Parasitic Capacitance

Driving signal of TFT - LCD panel is divided into the data signal and gate signal, which drive grid electrode and source electrode of pixel TFT respectively. Gate lines and data lines respectively in different metal layers of TFT substrate. For 65 UHD products, gate lines located in the 1st metal layer, and the data lines is located in the 2nd metal layer, the two metal layers are in the interval with a layer of insulating. In this way, the data lines and the gate lines overlap can form overlap parasitic capacitance. In addition to the overlap capacitance, there are data lines and COM lines overlap capacitance, forming reason is similar to the above. Every change of the data signal will be carried out on the overlap capacitance charging or discharging of action, influence the charging or discharging within the Pixel.

For general TFT - LCD Panel, the capacity value of data Line overlap capacitances is far greater than that in pixels, which is Cst (Storage Capacitor) and Clc (Liquid Crystal Capacitor). For example, 65 UHD products, Cst

= 0.78 pF, $C_{lc} = 0.2 \text{ pF}$, C_{oc} (single data line overlap capacitance) = 127 pF. So, we can say that, the main influence to the Data Load is overlap capacitance.

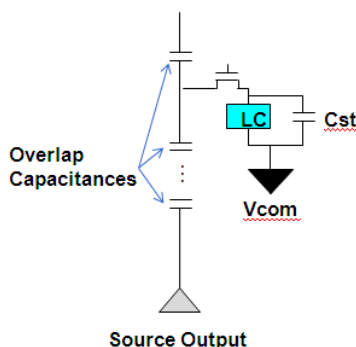


Fig. 1. Overlap Capacitances

2.2. The Influence of Data Rising and Falling Time

In the process of Source Driver IC output driving voltage, at the time of data rising, AVDD provide the driving power; at the time of data falling, GND provide the driving power;. Because of the difference of AVDD voltage setting and AVDD transient effects in the process of loading change, lead to the data output up and down time is not the same.

With 65 UHD panel as an example, cause of the 2G2D driven architecture, each data line in the same polarity within the same frame. When the panel show checker pattern with black and white, only in black and white handover location, data signal mutation is produced (up or down). Under the influence of the load within a panel, AVDD current can increase instantaneously, causing AVDD voltage reduced, as shown in Fig. 2, exacerbated the differences between the actual rising and falling time in output data.

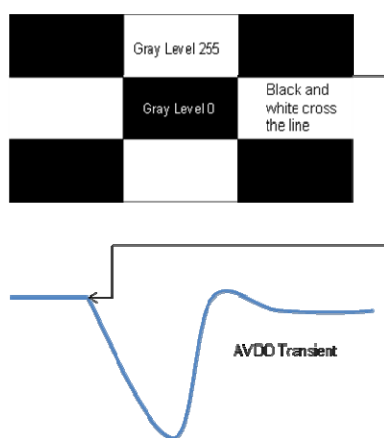


Fig. 2. AVDD Transient

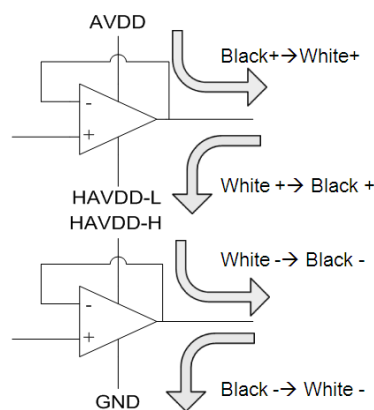


Fig. 3. HAVDD Structure

2.3. The Influence of HAVDD

Considering of power saving, the large size, high resolution TFT-LCD Panel mainly adopt HAVDD structure, as shown in Fig. 3.

According the structure of Source Driver IC, it will divided into HAVDD-L and HAVDD-H inside, which is used for discharging Gamma+ voltage and charging Gamma- voltage. When adopt HAVDD structure in 65UHD ADS mode product, which is normally black, at the time of picture Black+→White+, panel will charge from AVDD; In a similar way, at the time of picture White+→ Black+, panel will discharge from HAVDD-L; At the time of picture White-→ Black-, panel will charge from HAVDD-H; At the time of picture White+→ Black+, panel will discharge from GND.

3. Experiments and Results

Based on the principle of the above analysis, this paper mainly adopts 65 UHD ADS products, using timing adjustment and debugging HAVDD voltage, improve line image sticking:

3.1. Timing Adjustment

Due to the large size, high resolution products suffer from long-term insufficient charge rate, when timing is set, to do our best to increase the gate opening time, extend the charging time. But in this way, the data signal increase or decrease period will influence the final filling voltage in the pixel.

As shown in Fig. 4 and Fig. 5, Gate n displayed white, and the line up to Gate n displayed black, in order to prevent the happening of the charging error, after a period of Gate n opened, began to change the data, this time to charge the the overlap capacitance on data line and Cst & Clc in pixel charging at the same time. Due to the above analysis of Source Driver IC charge, discharge difference, will cause different positive and negative charging rate in this area. When Gate n+1 opened, data voltage keep steady, is no longer affected by data up and down. Thus result in black and white border area and Normal area different charging and discharging properties, line image sticking appeared.

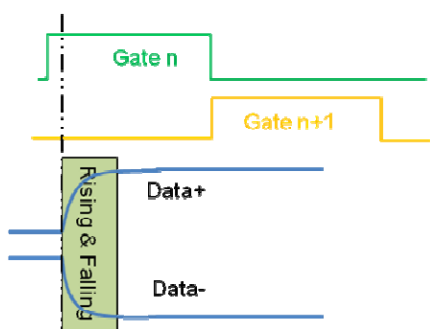


Fig. 4. Normal Timing (Black→White)

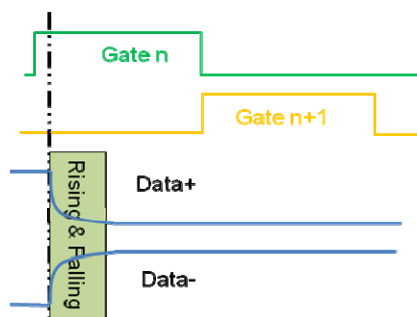


Fig. 5. Normal Timing (White→Black)

Consider the analysis in section 2, mainly influencing the charge and discharge factors is data overlap capacitance on the data line. So, as shown in Fig. 6 and 7, at the time of the data changes, through OE signal control, to make all the Gate is closed, so that, after the Source Driver IC have charged the overlap capacitances on data line, signal basic remained stable, open the Gate, charge pixels inside. As we do that, we can basically keep charge ratio the same level in different area, to reduce or eliminate line image sticking.

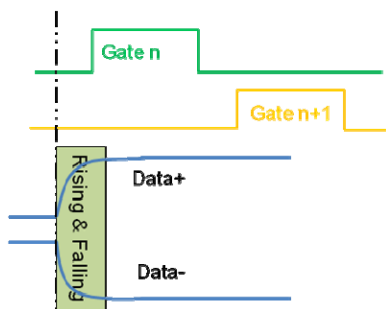


Fig. 6. Improve Timing (Black→White)

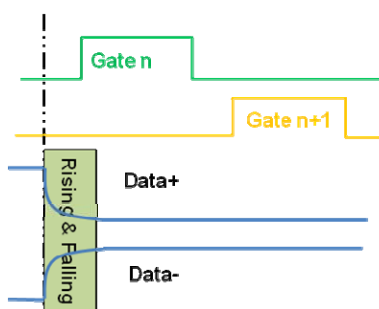


Fig. 7. Improve Timing (White→Black)

Table 1. OE Time & Line Image Sticking

| OE Time | Line Image Sticking |
|---------|-------------------------|
| 0.2us | 0.5h Appear |
| 0.7us | 1h Appear |
| 1.2us | 168h without Appearance |

As shown in Table 1, OE time were 0.2 us, 0.7 us, 1.2 us, can be found that increase OE time can significantly improve line imager sticking. But this method will bring some other side effect, which could reduce pixels charging time, reduce charging rate.

3.2. HAVDD Adjustment

As a result of Timing adjustment will reduce pixels charging time, so, further highlight the problem of insufficient charge ratio, so add the HAVDD adjustment, reduce the OE time as far as possible, increase the charging time.

According to the discussion of section 2.3, HAVDD voltage can influence the Source Driver IC output driving capability, which affects the data up and down time.

As shown in Fig. 8 and Fig. 9, before adjustment of HAVDD, rising and falling time is 1179 ns and 753 ns, after adjustment is 386 ns and 401 ns.



Fig. 8. Before HAVDD Improve

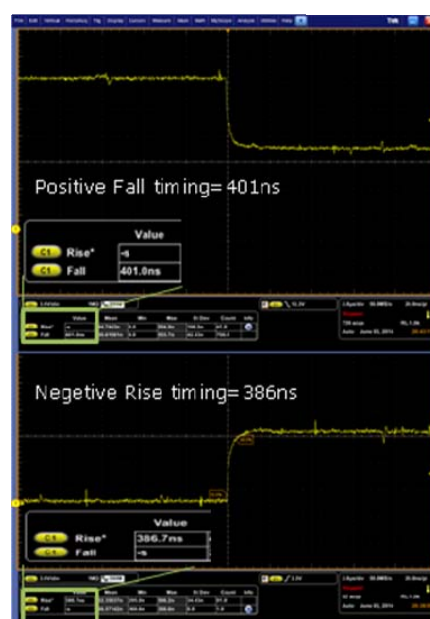


Fig. 9. After HAVDD Improve

After HAVDD debugging, at the condition of OE=0.2us, line image sticking was not appeared in 168h, increasing the charge ratio of product.

4. Impact

In this paper, the reasons of large size, high resolution product line image sticking are discussed, the three influence factors are proposed: the influence of parasitic capacitance; the influence of data rising and falling time; the influence of HAVDD. The paper in addition provides a feasible improvement measures for the large size, high resolution product line image sticking problems: Timing adjustment and debugging HAVDD voltage. The experimental results show the effectiveness of the two methods and prove the solutions.

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6. References

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