Study on Improvement of the Leakage-like Defect Problems in OLED Panel by Off-current Control of the Driving TFTs

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Low temperature poly silicon(LTPS) process has been introduced widely as a backplane technology of the organic light-emitting diode(OLED) displays. For implementation to high-resolution OLED displays, demand on the higher mobility for the pixel driving TFT is increased. In most of OLED backplanes using co-planar structure TFT layout, a relatively thinner gate insulator for TFT is essential to improve the mobility. However, as thinning the gate insulator, the leakage current of the pixel driving TFT(I_{off}) can be increased, and this results in higher risk on the week bright-dot defect problems on OLED displays. To reduce I_{off}, a LDD(lightly doped drain) TFT structure [1,2] and a multi-gate TFT structure [3] are proposed. However, these methods need additional process steps or result relatively low aperture ratio.

In this study, an off-state-bias-stress(OSBS) method has been introduced to improve the TFT leakage-current without changing the backplane structure or additional process steps. During the defect checking step in backplane process, by applying OSBS voltages to the TFTs as shown in Fig. 1, the I_{off} can be reduced effectively as shown in Fig. 2. Under the suitable OSBS condition, electrons are bounded in the gate insulator and this effect results in lower GIDL(gate induced drain leakage) by effectively reduced gate electric-field. In this method, V_{th} shift can be resulted if V_{gs} is higher than 30 volts, and V_{ds} change results in no V_{th} shift. I_{off} current can be minimized without V_{th} shift by minimizing V_{gs} and adjusting V_{gd} during OSBS.

As a result, weak-bright dots and low-gray-mura defects of the OLED display due to leakage-current of the driving TFT can be reduced dramatically by OSBS.

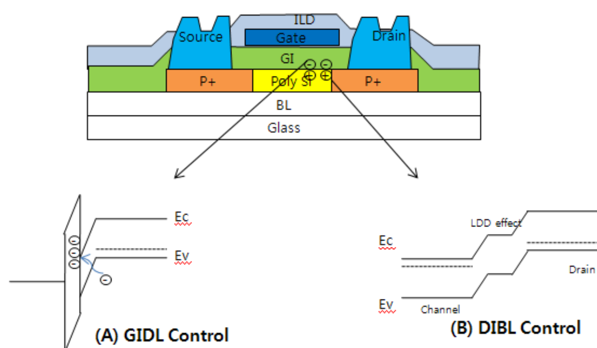

Fig. 1. Mechanism of OSBS on TFT

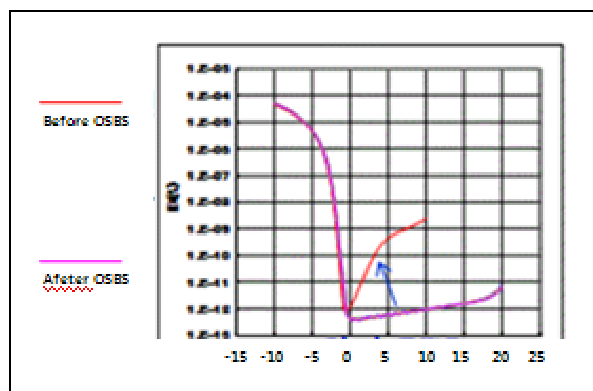

Fig. 2. Effect of OSBS on I-V characteristics

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