Reduction of leakage current of poly-Si TFTs with metal source/drain by dual gate structure

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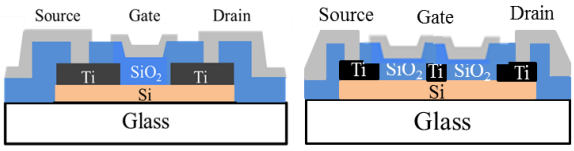
LTPS (Low Temperature Poly-Silicon) TFTs (Thin Film Transistors) with high mobility have a number of advantages for O-LED (Organic-Light Emitting Diode) pixel and for LCD (Liquid Crystal Display) such as low power consumption and integrating functional circuits on a panel. Recently, BLDA (Blue Laser Diode Annealing) was reported as a next generation LTPS process. BLDA can heat up the thin Si film uniformly by slightly deeper penetration depth than UV laser and is expected to obtain uniform grain size with reduced surface roughness [1]. Also, our group has proposed and shown simple TFT structure with metal source/drain without using impurity doping [2]. Although Si TFT with metal source/drain of Ti is expected to reduce the fabrication cost [2], leakage current seems to be rather higher than conventional doped source/drain. Dual-gate TFT structure of series connection is expected to be effective for reducing the off leak current [3].

Top gate structured poly Si TFTs using BLDA have been fabricated on glass substrates. For the TFT fabrication, channel Si layer of 50 nm thickness was deposited by PE CVD and subsequently dehydrogenated at 490˚C. The beam size was controlled at 600×2.4 μm^2 and the Si films were crystallized by BLDA at 5 W. After patterning the Si film for TFT channel, subsequent hydrogenation at 400˚C for 60 min. Ti as a metal source/drain was deposited using vacuum evaporation. After patterning the Ti film, SiO_2 film of 100 nm thickness was deposited as a gate insulator at room temperature using RF sputtering. After patterning the SiO_2 for contact holes, Al electrodes were evaporated. Finally, the TFT was annealed at 400˚C for 60 min in H_2/N_2 (4%) atmosphere to reduce the defects in Si and Si/SiO_2 interface. Besides of TFT fabrication, device simulation for the conventional structured poly-Si TFT has been conducted as a comparison.

Fig.1 shows cross-sectional view of single gate and dual gate TFT. Fig.2 shows transfer curves of poly Si TFT (L/W = 20 μm/5 μm, V_d = 1 V) after H_2 annealing for 60 min. Considerable reduction of off leak current for dual gate structure is observed. In conventional n^+ source/drain structure, the effect of the leakage reduction was also observed by simulation.

By applying the dual gate structure for the LTPS TFT with metal source/drain structure, reduction of leakage current which affects to stable driving with saving power is expected.



(a) Single gate, (b) Dual gate

Fig.1 Cross-sectional view of TFT

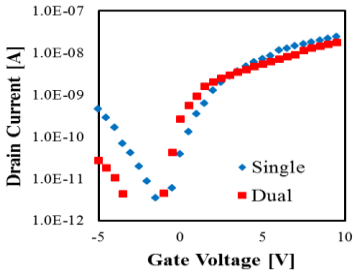


Fig.2 TFT characteristics after H_2 annealing at 400˚C for 60 min

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